REMARKS

The Examiner is thanked for the opportunity to discuss this application during the Examiner Interview on August 27, 2004.

1. Summary of the Office Action

Claims 12-16 stand rejected under 35 U.S. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

Claims 1-10 and 12-31 stand rejected under 35 U.S. 103(a) as allegedly being unpatentable over U.S. Serial No. 5,717,617 (Chester) in view of U.S. Serial No. 5,786,778 (Adams).

Claims 11, 22, 31, and 32 stand rejected under 35 U.S. 103(a) as allegedly being unpatentable over Chester in view of Adams and in further view of U.S. Serial No. 5,808,924 (White).

2. Response to § 112 Rejection

Claim 12 reads as follows:

> **A method** for converting a digital audio signal to a different sample rate, **the method** comprising…

It is submitted that "the method" in the second line does in fact have antecedent basis and withdrawal of this rejection is earnestly requested.

3. Response to § 103 Rejections

To establish a **prima facie** case of **obviousness**, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicant respectfully traverses this rejection for the reasons set out below, and asks the Examiner for reconsideration. The applicant's response to the rejections is addressed as follows:

1. An overview of Adams making salient points regarding the nature of this invention.
2. An overview of Chester, including a discussion of multi-rate signal processing and the nature of this invention.
3. Comments on the submission in the Office Action with respect to the manner in which Chester and Adams might be combined, including the motivation for such combination.
4. A demonstration that the references Chester and Adams cannot be usefully combined, comprising three points:
    a. If the circuitry of Adams can be placed after that of Chester, such that the output of Chester is connected to the input of Adams, the resulting combination has no utility.
    b. If the circuitry of Adams can be placed before that of Chester, such that the output of Adams is connected to the input of Chester, the resulting combination has no utility.

c. Placing the circuitry of Adams within that of Chester, such that an intermediate output of Chester is connected to the input of Adams, and the output of Adams is connected to an intermediate input of Chester, could not be accomplished by one skilled in the art.

It submitted that these arguments, as discussed below, clearly demonstrate that the inventions of Adams and Chester cannot be combined in any meaningful manner that it would **not** be obvious to a person of ordinary skill in the art to combine their teachings.

1. An overview of Adams

Adams provides a real-time signal processing circuit which accepts a digital signal clocked at a periodic sample rate Fs, and provides an output signal clocked at an instantaneously variable rate whose average rate is an integer multiple of the incoming sample rate. This output signal clock is produced by a noise-shaped DCO within Adams, and produces a "jittery" version of the interpolated input signal. The output signal clock, while "jittery," has edges that are always coincident with a master clock MCLK, whose rate is not required to be an integral multiple of the incoming sample rate. While the data sequence of the output signal is the same as the output of a conventional interpolator, when the output signal spectrum is analyzed by considering it as instead a fixed sample rate signal at the MCLK rate, it is found to be distortion free and representative of the incoming signal.

2. An overview of Chester

Chester provides a method for the conversion of sample rates by a rational ratio within a conventional multi-rate signal processing framework. Chester's input signal x(n) and output signal y(m) represent the same signal sampled at different rates, and Chester merely provides the mathematical algorithm for computing the output sample sequence y(m) at the new rate Fy = L/M * Fx based on the input sequence x(n) at rate Fx.

Chester provides no information with respect to the real-time implementation of his algorithms in digital hardware. Thus one of ordinary skill in the art must apply traditional techniques to implement Chester. There are basically three approaches. One can consider the input to Chester as one "file" (such as a ".wav" file of audio data on a computer), and the output as another such file, in which case the algorithms of Chester are applied to the input file (which was presumably captured at the sample rate Fx) and the output file ultimately converted to an analog signal at the output sample rate Fy. One can implement the algorithms of Chester in a digital signal processing computer (DSP chip) operating at such a speed that the input samples x(n) acquired at rate Fx are buffered, operated upon by the DSP, and the output samples y(m) produced in time and at a rate adequate that y(m) can then be output at rate Fy. Or one can build hardware in which input samples x(n) are sequentially stored in registers periodically clocked at rate Fx, computations performed in real time, and the results placed in registers periodically clocked at rate Fy, where Fy is exactly L/M times Fx. Any intermediate signal would similarly be stored in registers clocked at the appropriate intermediate rate.

3. Comments on the submission in the Office Action with respect to the manner in which Chester and Adams might be combined

The Office Action suggests "To one of ordinary skill in the art at the time of the invention, it would have been obvious to include a variable clock rate system for the clocking the interpolators and decimators of the system of Chester. The motivation behind such a modification would have been that such a system would have enabled the interpolator or decimator to accurately process the input samples in view of the variable sample rate of the signal, taking into account an average variation in the input sample rate relative to that of a master clock. In other words, such a system allows a variant input sample rate to still be accurately processed with a master input clock, wherein the input sample rate is not an integer multiple of the master clock rate. The various rate changes, as shown in figure 9, are considered herein to be the continuously varying output sample rate signals."

Including "a variable clock rate system for the clocking the interpolators and decimators of the system of Chester" clearly implies that the noise shaped clock signal 65 of Adams is to be used to clock the flip-flops holding the various inter-stage signals of Chester. It will be shown below that such a configuration is either non-obvious or not useful.

While "allow[ing] a variant input sample rate to still be accurately processed with a master input clock, wherein the input sample rate is not an integer multiple of the master clock rate" is possible (although please note that, more correctly stated, the master clock rate is not an integer multiple of the sample rate), but such processing is accomplished by placing Adams' circuitry entirely before that of Chester, so that, for example, an analog signal is converted into digital form at an sample rate that is not an integer multiple of the master clock rate. It will be shown below that in such a configuration, following Adams with Chester has no utility. In other words, it will be shown that the same result could be achieved more effectively by proper application of Adams alone.

When the Office Action suggests that "such a system would have enabled the interpolator or decimator to accurately process the input samples in view of the variable sample rate of the signal, taking into account an average variation in the input sample rate relative to that of a master clock", it is not entirely clear what is meant. If the Office Action is asserting that Adams somehow enables a system to take into account random variations in clock rate such as found in the real world, it should be noted that the invention of Adams itself creates the noise shaped clock signal, and thus does not respond in any way to an external clock having variations in rate. If on the other hand, the Office Action is suggesting that the circuitry in Adams be employed to create average variations in the input sample rate relative to a master clock, it is submitted that there is no utility in creating such variations purely for the point of having the circuitry properly process these varying signals. Further, it should be noted that the only processing block within Adams, the conventional interpolation filter 84, is described by Adams at column 8 lines 38-42, as producing the exact same numeric values as one operating at a fixed sample rate. Thus it should be clear that there is no change in the processing based on the variations in the sample rate, so the Office Action's suggestion that somehow Adams when added to

Chester would enable more accurate processing than what would occur with Chester alone is questionable.

When the Office Action states "[t]he various rate changes, as shown in figure 9, are considered herein to be the continuously varying output sample rate signals" it would seem to imply that the interpolated output signal 91, which is illustrated in figure 9, is considered the ultimate output signal. This would imply that Adams is being combined with Chester in such a manner that the circuitry of Adams is entirely subsequent to that of Chester. It will be shown below that in such a configuration, following Chester with Adams has no utility. In other words, it will be shown that the same result could be achieved more effectively by proper application of Adams alone.

In summary, the Office Action is not entirely clear as to how exactly Adams is meant to be combined with Chester. In the explanation below, it will be shown that when Adams either entirely precedes Chester or is entirely subsequent to Chester, there is no utility to the combination. It will be further shown that it is not possible for one of ordinary skill in the art to meaningfully and usefully combine Adams and Chester in such a manner that Adams is used within Chester.

4a. Placing Adams subsequent to Chester

One arguable way in which Adams could be combined with Chester is by placing Adams subsequent to Chester. A preferred embodiment of Chester, as shown in figure 9 of Chester, has an output y(m) that represents a signal at a particular sample rate that is a rational ratio L/M of the sample rate of the input signal x(n). Such an output, when embodied in hardware compatible with that of Adams, would comprise a data signal and a clock at the signal's sampling rate. This could be connected to the input of Adams, in a typical embodiment as illustrated in figure 9. Adams will accept the data signal on data bus 86, and the associated clock on the Fs IN signal 74. Adams may then convert this signal to a new signal having an average sample rate L'/M' (typically L=128, M=1)

clocked by a noise shaped clock coincident with a master clock MCLK running at a high rate (typically 27 MHz).

Adams states in column 1 lines 8-10 that "the present invention relates to a method and circuit for performing digital-to-analog signal conversion using continuously variable digital interpolation", and as shown in figure 3 and its corresponding explanation in column 5, lines 18-38 Adams invention primarily relates to Digital to Analog conversion. Adams further states in column 10 lines 22-24, "[i]n a typical oversampled sigma-delta DAC system, the interpolator is followed by a digital sigma-delta modulator, then by a DAC." It should be clear that Adams anticipates his invention for use within a Digital to Analog Converter, and that no other possible uses are described or even suggested.

One can thus view the alleged combination of Adams subsequent to Chester as the following: Chester accepts an input signal x(n) at a sample rate Fx, and converts it to a signal y(m) at a sample rate Fy, where Fy = Fx * L/M. Adams then converts signal y(m) to a new sample rate, typically at an average rate of 128*Fy, which is clocked coincident with a master clock MCLK running at a high rate, typically 27 MHz. Adams shows that the output signal is in a form useful for conversion to the analog domain.

It should be obvious to one of ordinary skill in the art that the utility of such a combination could have just as easily been accomplished using Adams alone. The input of the combination is a signal at a sample rate of Fx. The ultimate output of the combination is an analog signal, converted to the analog domain by hardware clocked by a master clock running at a particular rate, typically 27 MHz. Adams places no restriction on the incoming sample rate of the signal. Thus the signal being input to Adams could just as well have been x(n) as y(m). These both represent the same signal, and are just sampled at differing rates, so the output of Adams in either case represents the same exact signal. In either case, Adams can be clocked by MCLK at the desired rate, since there is no requirement for MCLK to be an integer multiple of Fx or Fy. **It should thus be clear that the combination of Adams subsequent to Chester has no**

utility over the utility of Adams alone, and thus there is no motivation to combine the inventions.

4b. Placing Adams preceding Chester

Another arguable way in which Adams could be combined with Chester is by placing Adams preceding Chester. A preferred embodiment of Chester, as shown in figure 9 of Chester, has an input x(m) that represents a signal at a particular sample rate. Such an input, when embodied in hardware compatible with that of Adams, would comprise a data signal and a clock at the signal's sampling rate. This could be connected to the output of Adams, in a typical embodiment as illustrated in Adams figure 13. Adams will produce the data signal on DOUT bus 136, which is sampled at the fixed periodic rate determined by the Fs CLOCK signal 74. Adams thus begins with a presumably analog signal, which is then presumable sampled from the analog at the precisely periodic 27 MHz MCLK rate, in signal source 140. The noise-shaped clock 65 then produces a new signal having an average sample rate L'/M' (typically L=128, M=1) times the FS CLOCK rate, which is then decimated to form the strictly periodically sampled signal x(n) at a rate Fx as set by FS CLOCK. Signal x(n) is now applied to Chester for rate conversion to a new signal y(m) at a sample rate rate Fy where Fy = L/M * Fx.

Adams states in column 1 lines 8-12 that "the present invention relates to a method and circuit for performing … analog-to-digital conversion using decimation." It should be clear that Adams anticipates the figure 13 embodiment of his invention for use within a Analog to Digital Converter, and that no other possible uses are described or even suggested.

One can thus view the alleged combination of Adams preceding Chester as the following: Adams accepts an analog signal, and samples it periodically at the high rate of the master clock MCLK, typically 27 MHz. Adams then selects certain of these samples to produce a signal with an average rate that is a rational multiple of the output rate Fx of Adams, typically 128*Fx. Adams applies these selected samples to a decimation filter to produce

an output signal x(n) at a strictly periodic sample rate Fx. Chester accepts the signal x(n) at the sample rate Fx, and converts it to the output signal y(m) at a sample rate Fy, where Fy = Fx * L/M.

It should be obvious to one of ordinary skill in the art that the utility of such a combination could have just as easily been accomplished using Adams alone. The input of the combination is an analog signal, which is then periodically sampled at a high rate by the master clock MCLK. The ultimate output of the combination is periodically sampled digital signal y(m) at a sample rate Fy. Adams places no restriction on the output sample rate of his invention. Thus the signal being output by Adams could just as well have been y(n) at the rate Fy as x(m) at the rate Fx. These both represent the same signal, and are just sampled at differing rates, so the output of Adams in either case represents the same exact signal. In either case, Adams can be clocked by MCLK at the desired rate, since there is no requirement for MCLK to be an integer multiple of Fx or Fy. **It should thus be clear that the combination of Adams preceding Chester has no utility over the utility of Adams alone, and thus there is no motivation to combine the inventions.**

4c. Placing Adams to act as an intermediate stage of Chester

In order to combine Adams and Chester in such a manner that Adams serves as an intermediate stage to Chester, one must connect the output of one of Chester's stages to the input of Adams, and the output of Adams to the input of a subsequent stage of Chester.

A typical embodiment of Chester is illustrated in Chester's figure 9. As possible argument, consider replacing the 3rd stage of Chester with an embodiment of Adams. As noted above, any of Chester's intermediate signals represent periodically sampled digital signals, and as such, correspond in hardware compatible with Adams as a data signal and a corresponding periodic clock at the associated sample rate of the data signal. Thus in order to connect Adams to the intermediate stages of Chester, one must supply to Adams

as input a data signal and the corresponding periodic clock at the input sample rate, and obtain from Adams as output a data signal and the corresponding periodic clock at the output sample rate.

Selecting Adams' preferred embodiment as shown in Adams figure 8, the manner in which to connect the output of Chester's LPF2 as an input to Adams should be obvious. Since the output of LPF2 has a data signal (which we shall call w, this can be connected to Adams' data input 86, and LPF2 has a clock signal with a fixed period at the output sample rate of LPF2 (let us call this Fw) which would be connected to Adams' FS IN terminal 74.

Adams produces an output signal (which we shall call z). As explained in column 3, lines 39-42 of Adams, the output is "a noise-shaped clock signal having a "variable rate" (instantaneously variable) with an average rate equal to an integer multiple of the input sample rate" and (from column 3 line 46) "interpolated output samples at the variable rate." It is thus clear that the clock for the output signal z of Adams is the noise shaped clock 65 of figure 8 operating at an average sample rate Fz = L'/M' * Fx, and the signal z is the output 88 of interpolation filter 84.

Adams points out, in column 8 line 42-46, that with respect to this signal "[t]he output sequence must be considered to be a discrete-time sequence at the full master clock rate M_{clk}" but for the purposes of the Office Action's arguments the master clock MCLK cannot be considered the clock output of Adams at the output signal's sample rate for application to the next stage of Chester. This should be clear for two reasons. The first is that Adams has clearly stated that the output signal has a variable rate with an average rate equal to an integer multiple of the input sample rate. The master clock MCLK operates at a fixed 27 MHz rate in the typical embodiment, clearly not an integer multiple of the sample rate, and just as clearly not a variable rate as well. Second, the Office Action's arguments hinge entirely around the production of a signal at a variable sample rate, in fact one that is "instantaneously variable." Since the input to Adams from Chester by necessity is at a fixed and periodic sample rate, and if the output of Adams

into Chester is operating at a fixed and periodic rate of M_{clk} (typically 27 MHz), there exists no instantaneously variable sample rate signal and the Office Action's submission that the invention reads on applicant's claims must be rejected.

Thus for the Office Action's arguments to be effective, one of ordinary skill in the art must try and find a way to usefully connect the outputs 88 and 65 of Adams figure 8 into Chester. This presents a problem, because Chester has been designed to process signals having a periodic sample rate.

One might naively suggest that the noise-shaped clock of Adams on line 65 simply be propagated through the remainder of Chester. While (considering figure 9 of Chester) stage 4 (LPF4) could be so operated, it must be remembered that stage 5 is a multirate stage and thus produces M1 output samples for every Mx input samples. Thus the clock rate at the output y(m) of Chester will not operate at the same rate as its input, but at M1/Mx times that rate. It is submitted that there is no guidance for one of ordinary skill in the art to create such a clock based on Adams signal 65, and its production on such a basis would be far from obvious. And if the output clock at rate Fy for signal y(m) is not based on Adams' signal 65, then the variable sample rate of Adams has no impact on the signal processing. Since the Adams stage produces a sequence of numbers that is the same as a conventional interpolation filter (Adams column 8 lines 38-42), the effect of Adams on the signal is contained purely in the timing of clock 65. If the subsequent circuitry ignores this clock, then the output of Adams will have the same consequences as a strictly periodic signal of that rate.

The only alternatives for the use of Adams' clock signal 65 within Chester are to ignore it or in some way to use the clock signal to alter the data in a manner that provides corrected values at a strictly periodic clock rate. Ignoring noise-shaped clock 65, as discussed above, will mean that Adams is no different than Chester's original stage. It is submitted that using the clock signal to operate on the data is something not suggested by the references cited and far from obvious to one of ordinary skill in the art.

It has thus been shown that the incorporation of Adams as an intermediate stage of Chester is not something that could be accomplished by one of ordinary skill in the art. This, based with the results further above, clearly show that Adams cannot be usefully combined with Chester in any useful manner.

4. <u>Conclusion</u>

Having tendered the above remarks, Applicant respectfully submits that all rejections have been addressed and that the claims are now in a condition for allowance, which is earnestly solicited.

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact Garth Vivier at (408) 947-8200 ext. 245.

Respectfully submitted,
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Dated: 09/02/ 2004

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